Blank

|  |  |
| --- | --- |
|  |  |
|  |
|  |
|  |
|  |

State in between S1 and S2 to send R7 to PC also ensure in regfile

1. ADD

|  |  |
| --- | --- |
| PC -> mem\_a,alu\_a  +1 -> alu\_b  mem\_d -> ir  alu\_out -> PC |  |
|  |
|  |
| S1 |
|  |
| ir(0-8) -> SE9  ir(9-11) -> rf\_a1  ir(6-8) -> rf\_a2  rf\_d1 -> t1  rf\_d2 -> t2  ir(0-6)->SE6(not reqd, no sense, for ADI,BEQ) | NA |
| None |
| No flag |
| S2 |
| S3 |
| t1 -> alu\_a  t2 -> alu\_b | NA |
| ADD(or AND decided by opcode) |
| Z,C |
| S3 |
| S4 |
| OP -> rf\_d3  ir(3-5) -> rf\_a3 | NA |
| None |
| No flag |
| S4 |
| S1 |

1. ADC

|  |  |
| --- | --- |
| PC -> mem\_a,alu\_a  +1 -> alu\_b  mem\_d -> ir  alu\_out -> PC |  |
|  |
|  |
| S1 |
|  |
| ir(0-8) -> SE9  ir(9-11) -> rf\_a1  ir(6-8) -> rf\_a2  rf\_d1 -> t1  rf\_d2 -> t2  ir(0-6)->SE6(not reqd, no sense, for ADI,BEQ) |  |
|  |
|  |
| S2 |
|  |

If carry go to S3 else S1. ----------------------- need decoder after S2

1. ADZ

|  |  |
| --- | --- |
| PC -> mem\_a,alu\_a  +1 -> alu\_b  mem\_d -> ir  alu\_out -> PC |  |
|  |
|  |
| S1 |
|  |
| ir(0-8) -> SE9  ir(9-11) -> rf\_a1  ir(6-8) -> rf\_a2  rf\_d1 -> t1  rf\_d2 -> t2  ir(0-6)->SE6(not reqd, no sense, for ADI,BEQ) |  |
|  |
|  |
| S2 |
|  |

If zero go to S3 else S1, ---------------------- need decoder after S2.

1. ADI

|  |  |
| --- | --- |
| PC -> mem\_a,alu\_a  +1 -> alu\_b  mem\_d -> ir  alu\_out -> PC |  |
|  |
|  |
| S1 |
|  |
| ir(0-8) -> SE9  ir(9-11) -> rf\_a1  ir(6-8) -> rf\_a2  rf\_d1 -> t1  rf\_d2 -> t2  ir(0-6)->SE6(not reqd, no sense, for ADI,BEQ) |  |
|  |
|  |
| S2 |
|  |
| t1 -> alu\_a  SE6 -> alu\_b | NA |
| ADD |
| Z,C |
| S5 |
| S6 |
| OP -> rf\_d3  ir(6-8) -> rf\_a3 | NA |
| None |
| No flag |
| S6 |
| S1 |

1. NDU

|  |  |
| --- | --- |
| PC -> mem\_a,alu\_a  +1 -> alu\_b  mem\_d -> ir  alu\_out -> PC |  |
|  |
|  |
| S1 |
|  |
| ir(0-8) -> SE9  ir(9-11) -> rf\_a1  ir(6-8) -> rf\_a2  rf\_d1 -> t1  rf\_d2 -> t2  ir(0-6)->SE6(not reqd, no sense, for ADI,BEQ) |  |
|  |
|  |
| S2 |
|  |
| t1 -> alu\_a  t2 -> alu\_b |  |
| AND |
|  |
| S3 |
|  |
| OP -> rf\_d3  ir(3-5) -> rf\_a3 |  |
|  |
|  |
| S4 |
| S1 |

1. NDC

After S2, if carry AND operation in S3(ALU) else S1

1. NDZ

After S2, if zero AND operation in S3(ALU) else S1

1. LHI

|  |  |
| --- | --- |
| PC -> mem\_a,alu\_a  +1 -> alu\_b  mem\_d -> ir  alu\_out -> PC |  |
|  |
|  |
|  |
| S1 |
|  |
| ir(0-8) -> SE9  ir(9-11) -> rf\_a1  ir(6-8) -> rf\_a2  rf\_d1 -> t1  rf\_d2 -> t2  ir(0-6)->SE6(not reqd, no sense, for ADI,BEQ) | NA |
|  |
| None |
| No flag |
| S2 |
| S7 |
| SE9 -> rf\_d3  ir(9-11) -> rf\_a3 | NA |
| None |
| No flag |
| S7 |
| S1 |

1. LW

|  |  |
| --- | --- |
| PC -> mem\_a,alu\_a  +1 -> alu\_b  mem\_d -> ir  alu\_out -> PC |  |
|  |
|  |
| S1 |
|  |
| ir(0-8) -> SE9  ir(9-11) -> rf\_a1  ir(6-8) -> rf\_a2  rf\_d1 -> t1  rf\_d2 -> t2  ir(0-6)->SE6(not reqd, no sense, for ADI,BEQ) | NA |
| None |
| No flag |
| S2 |
| S9 |
| t2 -> alu\_a  SE6 -> alu\_b | NA |
| ADD |
| Z,C |
| S9 |
| S10 |
| OP -> datamem\_a  datamem\_dr -> rf\_d3  ir(9-11) -> rf\_a3 | Data read |
| None |
| No flag |
| S10 |
| S1 |

1. SW

S1 -> S2 -> S9 -> S10 -> S1

|  |  |
| --- | --- |
| OP -> datamem\_a  t1 -> datamem\_dw | Data write |
| None |
| No flag |
| S11 |
| S1 |

1. LM

|  |  |
| --- | --- |
| PC -> mem\_a,alu\_a  +1 -> alu\_b  mem\_d -> ir  alu\_out -> PC |  |
|  |
|  |
| S1 |
|  |
| ir(0-8) -> SE9  ir(9-11) -> rf\_a1  ir(6-8) -> rf\_a2  rf\_d1 -> t1  rf\_d2 -> t2  ir(0-6)->SE6(not reqd, no sense, for ADI,BEQ) |  |
|  |
|  |
| S2 |
|  |
| Ir(0-8) or pr\_en\_out-> PE / Shifter  rf\_d1 -> Address Incrementor | NA |
| None |
| No flag |
| S12 |
| S13(if not done LM ) else S14( not done SM) else S1 |
| pr\_en\_addr -> data\_mem\_addr  pr\_en\_addr\_reg -> rf\_a3  data\_mem\_read -> rf\_d3  pr\_en\_out -> PE/shifter | NA |
| Increment |
| No flag |
| S13 |
| S12 |

1. SM

|  |  |
| --- | --- |
| PC -> mem\_a,alu\_a  +1 -> alu\_b  mem\_d -> ir  alu\_out -> PC |  |
|  |
|  |
| S1 |
|  |
| ir(0-8) -> SE9  ir(9-11) -> rf\_a1  ir(6-8) -> rf\_a2  rf\_d1 -> t1  rf\_d2 -> t2  ir(0-6)->SE6(not reqd, no sense, for ADI,BEQ) |  |
|  |
|  |
| S2 |
| S12 |
| Ir(0-8) or pr\_en\_out-> PE / Shifter  rf\_d1 -> Address Incrementor |  |
|  |
|  |
| S12 |
| S13(if not done LM)else S14(not done SM) else S1 |
| pr\_en\_addr -> data\_mem\_addr  pr\_en\_addr\_reg -> rf\_a2  rf\_d2 -> data\_mem\_write  pr\_en\_out -> PE/shifter | Data write |
| None |
| No flag |
| S14 |
| S12 |

13. BEQ

|  |  |
| --- | --- |
| PC -> mem\_a,alu\_a  +1 -> alu\_b  mem\_d -> ir  OP -> PC |  |
|  |
|  |
| S1 |
|  |
| ir(0-8) -> SE9  ir(9-11) -> rf\_a1  ir(6-8) -> rf\_a2  rf\_d1 -> t1  rf\_d2 -> t2  ir(0-6)->SE6(not reqd, no sense, for ADI,BEQ) |  |
|  |
|  |
| S2 |
| S15 |
| t1 -> alu\_a  t2 -> alu\_b | NA |
| ADD(or AND or equality decided by opcode) |
| Z,C flag |
| S15 |
| if zero S16 else S1 |
| PC -> alu\_a  SE6 -> alu\_b  alu\_out -> PC | NA |
| ADD |
| No flag |
| S16 |
| S1 |

14. JAL

|  |  |
| --- | --- |
| PC -> mem\_a,alu\_a,(T)  +1 -> alu\_b  mem\_d -> ir  OP -> PC |  |
|  |
|  |
| S1(modified) |
|  |
| ir(0-8) -> SE9  ir(9-11) -> rf\_a1  ir(6-8) -> rf\_a2  rf\_d1 -> t1  rf\_d2 -> t2  ir(0-6)->SE6(not reqd, no sense, for ADI,BEQ) | NA |
| None |
| No flag |
| S2 |
| S17 |
| PC -> rf\_d3,alu\_a  ir(9-11) -> rf \_a3  SE9 -> alu\_b  alu\_out -> PC |  |
|  |
|  |
| S17 |
| S1 |

.

15. JLR

|  |  |
| --- | --- |
| PC -> mem\_a,alu\_a  +1 -> alu\_b  mem\_d -> ir  OP -> PC | NA |
| add |
| Z,C |
| S1 |
| S2 |
| ir(0-8) -> SE9  ir(9-11) -> rf\_a1  ir(6-8) -> rf\_a2  rf\_d1 -> t1  rf\_d2 -> t2  ir(0-6)->SE6(not reqd, no sense, for ADI,BEQ) | NA |
|  |
| None |
| No flag |
| S2 |
| S19 |
| ir(9-11) -> rf\_a3  PC -> rf\_d3  ir(6-8) -> rf\_a2  rf\_d2-> t2 |  |
|  |
|  |
| S19 |
| S20 |
| T2 -> PC |  |
|  |
|  |
| S20 |
| S1 |